Dolphin Technology

DOLPHIN TECHNOLOGY PRODUCT OFFERING
EMMC/SD/SDIO I2C/I2S

Dolphin Technology maintains a broad portfolio of SoC building blocks that provide silicon proven IP for customers who need It can be customized to support specific design requirements

EMMC/SD/SDIO – PHY & CONTROLLER	4/5/6/7 nm	12/16 nm	28nm	40nm	55nm	65nm
Compliant with eMMC 5.1, SD 4.1 and SDIO 4.1 Specifications	●	●	●	●	●	●
Transfers data in HS400, HS200, DDR52, SDR52 compatibility modes	●	●	●	●	●	●
Supports HS400, HS200, DDR52 and SDR52 data transfer modes	●	●	●	●	●	●
Supports UHS-II (SD 4.0) data transfer rates up to 312MB/s	●	●	●	●	●	●
Supports UHS-I (SD 3.01) data transfer rates up to 104MB/s	●	●	●	●	●	●
Supports 32-bit and 64-bit system data bus and addressing	●	●	●	●	●	●
Tuning for HS200 mode	●	●	●	●	●	●
4KB block support	●	●	●	●	●	●
32 bit DMA interface	●	●	●	●	●	●
Interrupts and wake up functionality	●	●	●	●	●	●
Supports both Asynchronous and Synchronous AXI4 Interface	●	●	●	●	●	●
AXI4 Narrow Transfer	●	●	●	●	●	●
Enhanced strobe function for reliable operation at HS400 mode.	●	●	●	●	●	●
Host clock rate variable between 0 and 200 MHz	●	●	●	●	●	●
Transfers the data in 1-bit, 4-bit and 8-bit modes	●	●	●	●	●	●
Supports Low-Power mode	●	●	●	●	●	●
Supports CUP/Wirebond and Flip Chip configurations	●	●	●	●	●	●
Precision master/slave digital DLL is used for timing circuits.	●	●	●	●	●	●
PHY uses 6 metal layers. Higher metals are configurable for improved power and ground mesh	●	●	●	●	●	●
PHY includes built-in DLL (50-200 MHz) to handle high-speed operations	●	●	●	●	●	●
IDDQ Model	●	●	●	●	●	●
PVT compensation	●	●	●	●	●	●
Power supplies include Core VDD, I/O VDD and VSS	●	●	●	●	●	●
No use of deep n-well devices	●	●	●	●	●	●
Interrupts and wake up functionality	●	●	●	●	●	●

I2C/I2S - PHY & CONTROLLER						
Drive programmable	●	●	●	●	●	●
Multi-mode support	●	●	●	●	●	●
Built in JTAG support for Mentor/LogicVision models	●	●	●	●	●	●
NAND or XOR tree select	●	●	●	●	●	●
Int/Out Register option	●	●	●	●	●	●
Pull down and sustain option	●	●	●	●	●	●
1.8 oxide	●	●	●	●	●	●
Metastability removal	●	●	●	●	●	●
Noise filter	●	●	●	●	●	●
Bus Start/Stop, stuck low detection	●	●	●	●	●	●
Signals (SDA/SCL) generation with user-defined timing constraints	●	●	●	●	●	●
Clock (SCL) synchronization	●	●	●	●	●	●

Front End views are available under NDA. For more information, click here or contact sales@dolphin-ic.com

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Bus arbitration	●	●	●	●	●	●
Customized I2C I/O:	●	●	●	●	●	●
• 1.8V / 2.5V oxide	●	●	●	●	●	●
• Multi-mode support	●	●	●	●	●	●
• Full power bus strapping based on metallization/top metal requirements (horizontal and vertical metallization option available from M6 and above)	●	●	●	●	●	●
• Available in Wirebond, Flip Chip and CUP configurations	●	●	●	●	●	●

DOLPHIN TECHNOLOGY PRODUCT OFFERING
DOLPHINWARE IP

Libraries	ASIC	FPGA
Data Integrity	●	●
Control Logic	●	●
Logic Component	●	●
FIFO	●	●
FIFO Controller	●	●
Arithmetic Component	●	●
Verification IPs	●	●
Memory BIST	●	●
Watchdog Timer	●	●
Real-time Clock	●	●
Triple time Clock	●	●
PVT monitor	●	
Temperature monitor	●	

Interfaces	ASIC	FPGA
JTAG Controller	●	●
UART/USART Controller	●	●
Serial Peripheral Interface Controller	●	●
Quad-Serial Peripheral Interface Controller	●	●
Octal- Serial Peripheral Interface Controller	●	●
Synchronous Serial Interface Controller	●	●
I3C Interface Controller	●	
General-purpose Input/Output Controller	●	●
Pulse Width Modulator Controller	●	●
Interrupt Controller	●	●
Convert SPI to I2C interface	●	●
Convert SPI to UART interface	●	●

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