Dolphin Technology

DOLPHIN TECHNOLOGY PRODUCT OFFERING
EMMC/SD/SDIO I2C/I2S

Dolphin Technology maintains a broad portfolio of SoC building blocks that provide silicon proven IP for customers who need It can be customized to support specific design requirements

EMMC/SD/SDIO – PHY&CONTROLLER	5/7 nm	12/16 nm	28nm	40nm	55nm	65nm
CompliantwitheMMC5.1,SD4.1 and SDIO4.1 Specifications	●	●	●	●	●	●
Transfersdata in HS400,HS200,DDR52,SDR52compatibility modes	●	●	●	●	●	●
SupportsHS400,HS200,DDR52 and SDR52 data transfermodes	●	●	●	●	●	●
SupportsUHS-II(SD4.0)data transferratesup to 312MB/s	●	●	●	●	●	●
SupportsUHS-I(SD3.01)data transferratesup to 104MB/s	●	●	●	●	●	●
Supports32-bitand 64-bitsystemdata busand addressing	●	●	●	●	●	●
Tuning forHS200 mode	●	●	●	●	●	●
4KBblocksupport	●	●	●	●	●	●
32 bitDMAinterface	●	●	●	●	●	●
Interruptsand wake up functionality	●	●	●	●	●	●
SupportsbothAsynchronousand SynchronousAXI4 Interface	●	●	●	●	●	●
AXI4 NarrowTransfer	●	●	●	●	●	●
Enhanced strobe function forreliable operation atHS400 mode.	●	●	●	●	●	●
Hostclockratevariable between 0 and 200 MHz	●	●	●	●	●	●
Transfersthe data in 1-bit,4-bitand 8-bitmodes	●	●	●	●	●	●
SupportsLow-Powermode	●	●	●	●	●	●
SupportsCUP/Wirebond andFlip Chip configurations	●	●	●	●	●	●
Precision master/slave digitalDLL isused fortiming circuits.	●	●	●	●	●	●
PHYuses 6 metallayers.Highermetals are configurable forimprovedpowerand ground mesh	●	●	●	●	●	●
PHYincludesbuilt-in DLL (50-200 MHz) to handle high-speed operations	●	●	●	●	●	●
IDDQModel	●	●	●	●	●	●
PVTcompensation	●	●	●	●	●	●
PowersuppliesincludeCore VDD, I/O VDDand VSS	●	●	●	●	●	●
No use ofdeepn-welldevices	●	●	●	●	●	●
Interruptsand wake up functionality	●	●	●	●	●	●

I2C/I2S - PHY&CONTROLLER						
Drive programmable	●	●	●	●	●	●
Multi-mode support	●	●	●	●	●	●
Builtin JTAG supportforMentor/LogicVisionmodels	●	●	●	●	●	●
NANDorXORtree select	●	●	●	●	●	●
Int/OutRegisteroption	●	●	●	●	●	●
Pulldown andsustain option	●	●	●	●	●	●
1.8 oxide	●	●	●	●	●	●
Metastabilityremoval	●	●	●	●	●	●
Noise filter	●	●	●	●	●	●
BusStart/Stop,stucklowdetection	●	●	●	●	●	●
Signals(SDA/SCL)generationwith user-defined timing constraints	●	●	●	●	●	●
Clock(SCL)synchronization	●	●	●	●	●	●
Busarbitration	●	●	●	●	●	●
Customized I2C I/O:	●	●	●	●	●	●

Front End viewsare available underNDA. For more information, click here or contact sales@dolphin-ic.com

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• 1.8V / 2.5Voxide	●	●	●	●	●	●	
• Multi-mode support	●	●	●	●	●	●	
• Fullpowerbusstrapping based on metallization/top metalrequirements(horizontalandverticalmetallizatio n option available from M6 and above)	●	●	●	●	●	●	
• Available inWirebond,Flip Chip and CUPconfigurations	●	●	●	●	●	●	

DOLPHIN TECHNOLOGY PRODUCT OFFERING
DOLPHINWARE IP

Libraries	ASIC	FPGA
Data Integrity	●	●
Control Logic	●	●
Logic Component	●	●
FIFO	●	●
FIFO Controller	●	●
Arithmetic Component	●	●
Verification IPs	●	●
Memory BIST	●	●
Watchdog Timer	●	●
Real-time Clock	●	●
PVT monitor	●	
Temperature monitor	●	

Interfaces	ASIC	FPGA
JTAG Controller	●	●
UART/USART Controller	●	●
Serial Peripheral Interface Controller	●	●
Quad-Serial Peripheral Interface Controller	●	●
Octal- Serial Peripheral Interface Controller	●	●
Synchronous Serial Interface Controller	●	●
I3C Interface Controller	●	
General-purpose Input/Output Controller	●	●
Pulse Width Modulator Controller	●	●
Interrupt Controller	●	●
Convert SPI to I2C interface	●	●
Convert SPI to UART interface	●	●

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